PHASE LOCKED LOOP LOCK-DETECTION CIRCUIT

ABSTRACT

[0028] An improved clock lock detection circuit is disclosed. The circuit has a first input indicating an edge of a first clock and a second input indicating a corresponding edge of a second clock wherein the second clock is expected to be synchronized with the first clock with an allowable time difference. Further, it has a difference generation module for generating a difference signal based on the time difference between the first and second inputs, and a voltage divider module for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs.

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